WHAT IS CLAIMED IS:

1. An UV-programmed P-type Mask ROM, comprising:

a heavily doped N-well in a substrate;

a plurality of bit lines in the heavily doped N-well;

an insulating layer on the bit lines;

a plurality of word lines crossing over the bit lines, wherein the substrate under a word line and between two bit lines serves as a memory cell;

a charge trapping layer between the word lines and the heavily doped N-well; and

an UV-blocking layer over the substrate having a plurality of openings over selected memory cells, wherein the selected memory cells are written by using UV light.

2. The UV-programmed P-type Mask ROM of claim 1, wherein a dopant of the heavily doped N-well comprises phosphorous.

3. The UV-programmed P-type Mask ROM of claim 1, wherein the selected memory cells written by using UV light store e-bit “1”.

4. The UV-programmed P-type Mask ROM of claim 1, wherein the charge trapping layer comprises a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer.

5. The UV-programmed P-type Mask ROM of claim 1, wherein the insulating layer comprises a thermal oxide layer.

6. The UV-programmed P-type Mask ROM of claim 1, wherein the UV-blocking layer comprises an UV-absorbable layer.

7. The UV-programmed P-type Mask ROM of claim 6, wherein the UV-

absorbable layer comprises an anti-reflection coating (ARC).

8. A method for fabricating an UV-programmed P-type Mask ROM, comprising the steps of:

forming a heavily doped N-well in a substrate;

forming a charge trapping layer on the substrate;

forming a plurality of bit lines in the heavily doped N-well;

forming an insulating layer on the bit lines;

forming a conductive layer on the substrate;

patterning the conductive layer to form a plurality of word lines crossing over the bit lines, wherein the substrate under a word line and between two bit lines serves as a memory cell;

forming an UV-blocking layer over the substrate, the UV-blocking layer having a plurality of openings therein over selected memory cells; and

writing the selected memory cells by using UV light.

9. The method of claim 8, wherein the selected memory cells store e-bit “1”.

10. The method of claim 8, wherein a dopant of the heavily doped N-well comprises phosphorous.

11. The method of claim 10, wherein an implanting energy for forming the heavily doped N-well is about 360KeV.

12. The method of claim 11, wherein an implanting dosage for forming the heavily doped N-well ranges from about $2.5\times10^{13}/cm^2$ to about $5\times10^{13}/cm^2$.

13. The method of claim 10, wherein an implanting energy for forming the heavily doped N-well is about 60KeV.

14. The method of claim 13, wherein an implanting dosage for forming the

heavily doped N-well ranges from about $5\times10^{12}/cm^2$ to about $9\times10^{12}/cm^2$.

15. The method of claim 8, wherein the charge trapping layer comprises a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer.

16. The method of claim 15, wherein a bottom oxide layer of the ONO composite layer serves as an etching termination layer for the step of patterning the conductive layer into the word lines.

17. The method of claim 8, wherein the insulating layer comprises a thermal oxide layer.

18. The method of claim 8, wherein the UV-blocking layer comprises an UV-absorbable layer.

19. The method of claim 18, wherein the UV-absorbable layer comprises an anti-reflection coating (ARC).

20. The method of claim 19, wherein the anti-reflection coating is formed by a method comprising chemical vapor deposition (CVD).